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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,643	12/01/2004	Fabrizio Campanale	CH 020020	8779
65913	7590	08/15/2007		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER RABOVIANSKI, ANTON I	
			ART UNIT 2188	PAPER NUMBER
			NOTIFICATION DATE 08/15/2007	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

**Office Action Summary**

Application No.

10/516,643

Applicant(s)

CAMPANALE, FABRIZIO

Examiner

Anton Rabovianski

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Status of Claims***

Claims 1-12 are pending in the Application.

Claims 1-12 have been amended.

Claims 1-12 are rejected.

### ***Response to Amendment***

Applicant's arguments filed 05/21/2007 have been fully considered but they are not persuasive. Therefore, the rejections made in the previous Office Action are maintained and restated, with changes as needed to address the amendments.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsai *et al.* (US 5,974,528).

With respect to claim 1, the Tsai *et al.* reference teaches a method for writing data from a processor (fig. 3, el. 310) to a non-volatile memory embedded in an integrated circuit (fig. 3, el. 330), comprising the following steps (a) at least part of said data to be written to said non-volatile memory is transferred to a volatile memory (col. 8,

lines 37-47), (b) when the part of said data has been transferred to said volatile memory, a wait signal is sent to said processor (col. 8, lines 48-50), (c) said part of said data is transferred from said volatile memory to said non-volatile memory (col. 8, lines 50-59), (d) said wait signal is removed (col. 8, lines 59-65).

Regarding claim 2, Tsai *et al.* further teach the data transfer to said volatile memory and to said non-volatile memory is controlled by an interface (col. 8, lines 37-47).

With respect to claim 3, Tsai *et al.* further disclose at the beginning of the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in write mode (col. 8, lines 37-62).

Regarding claim 4, Tsai *et al.* further disclose during the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in program mode (col. 8, lines 37-62).

Regarding claim 5, Tsai *et al.* further disclose at the end of the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in read mode (col. 8, lines 37-62).

Regarding claim 6, Tsai *et al.* further teach all of the data is transferred first to the volatile memory (col. 8, lines 37-47).

With respect to claim 7, Tsai *et al.* further disclose the addresses corresponding to the data to be written to the non-volatile memory are stored intermediately (col. 7, lines 41-48).

Regarding claim 8, Tsai *et al.* further teach before the data is written to the volatile memory, the wait signal is sent to the processor and is removed after said data is completely written to said volatile memory (col. 7, lines 49-67 and col. 8, lines 48-65).

With respect to claim 9, Tsai *et al.* disclose an integrated circuit with a processor (fig. 3, el. 310), a volatile memory (fig. 3, el. 340), a non-volatile memory (fig. 3, el. 330), and an interface connecting said processor to said volatile memory (fig. 3, el. 320), and said non-volatile memory to said volatile memory (fig. 3, el. 350), wherein said interface is equipped: to transfer data to be written to said non-volatile memory first to said volatile memory (col. 8, lines 37-47), to send a wait signal (wait) to said processor when said data is transferred to said volatile memory (col. 8, lines 48-50), to transfer said data from said volatile memory to said non-volatile memory (col. 8, lines 50-59), and to remove said wait signal (col. 8, lines 59-65).

Regarding claim 10, Tsai *et al.* further teach the non-volatile memory is a flash memory (col. 7, lines 41-44).

Regarding claim 12, Tsai *et al.* further disclose the volatile memory is an embedded volatile memory (fig. 3, el. 340).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai *et al.* (US 5,974,528) in view of Official notice.

With respect to claim 11, the Tsai *et al.* reference does not disclose the volatile memory is a random access memory or a static random access memory. However, RAM/SRAM are types of memories that are well known in the art, and Official notice of this is hereby taken. It would have been obvious at the time of the invention to a person having ordinary skill in the art to have modified the system disclosed by Tsai *et al.* to include RAM memory instead of register set so that more volatile storage is provided using less chip area.

### ***Response to Arguments***

Applicant argues that the Tsai reference teaches transferring data to a loader block of non-volatile memory and subsequently transferring data to a user block of non-volatile memory and thus not showing the limitations of claim 1. However, Tsai discloses writing data first to volatile memory in fig. 3, "register set" 340 and col. 8, lines 42-45 "new data are received via the I/O port 360 and transferred to the register set 340". Tsai also discloses transferring data from volatile memory to non-volatile memory in col. 8, lines 55-59. The reference also discloses that the microprocessor unit 310 goes into idle mode while data transfer is performed (col. 8, lines 48-50 and 59-62). Therefore, Tsai discloses all the limitations as claimed.

The well-known practices in the art in the rejection statement are considered admitted prior art because applicant failed to traverse the examiner's assertion of Official notice. See MPEP 2144.03.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anton Rabovianski whose telephone number is 571-270-1026. The examiner can normally be reached on M-Th 9:00am-7:30pm EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

Anton Rabovianski

July 27, 2007

  
HYUNG SOUGH  
SUPERVISORY PATENT EXAMINER  
8/01/07